Design Considerations for MMIC Distributed Amplifiers

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***Abstract*— The bandwidth of the input artificial line in a distributed amplifier is the main band limiting factor. By choosing this impedance properly the bandwidth of a distributed amplifier can be maximized. A four section GaAs MESFET distributed amplifier is designed using this strategy. The fabricated MMIC amplifier gives satisfactory performance. By adding proper length of series transmission lines in the drain side, the gain and the gain flatness of the amplifier can be further improved. This fact is presented via simulation results. The superior gain potential of cascode connected FETs is also demonstrated [2].**

1. INTRODUCTION

Distributed amplification is a way of adding device transconductances without adding device parasitic capacitances. In this amplification technique the input and output capacitances of the FETs are linked through inductors to form artificial transmission lines. The two artificial lines, the gate-line and the drain-line. are designed to match the load and source impedances in such a way that the return losses are above some specified limit. This limit is typically taken to be 10 dB. By optimizing the gate-line impedance the frequency band of the amplifier can be maximized. The typical structure of a distributed amplifier is shown in Fig. 1.

2. AMPLIFIER DESIGN GUIDELINES

An artificial line is a cascaded constant-k network. The characteristic impedance of an artificial line is given as,

$$Z_c(\omega) = Z_0 \times \sqrt{1 - \left(\frac{\omega}{\omega_c}\right)^2} \qquad (1)$$

where, $Z_0 = \sqrt{L/C}$ and $\omega_c = 2/\sqrt{LC}$.

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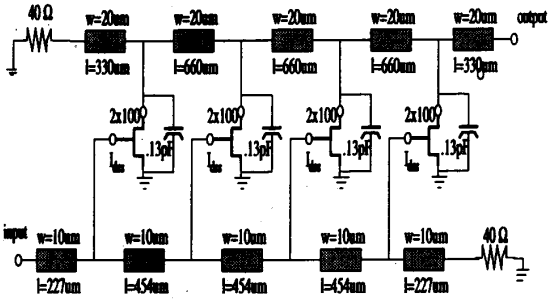

Fig. 1: Schematic of a Distributed Amplifier

When FETs are used as the active devices of distributed amplifiers, the artificial lines become lossy (Fig. 2). The gate-line contains a resistance in series with the capacitor, and the drain-line contains a conductance to the ground in parallel with the capacitor. The characteristic impedance expressions of these resistive artificial lines are more complicated.

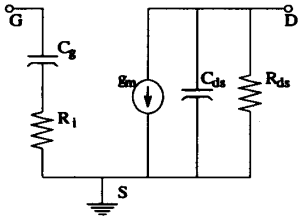

Fig. 2: Simplified model of a MESFET

For the gate-line, the series resistance can be neglected for frequencies at which the magnitude of the impedance of the capacitor is larger;

$$\frac{1}{\omega C_g} > R_i \Rightarrow \omega < \omega_g = \frac{1}{R_i C_g}.$$

For the drain-line, the shunt conductance can be ne-

glected for frequencies at which the magnitude of the conductance of the capacitor is larger;

$$\omega C_d > \frac{1}{R_{ds}} \Rightarrow \omega > \omega_d = \frac{1}{R_{ds} C_d}.$$

Then, the characteristic impedance of the gate and drain-lines can be approximated with the Eq. 1, for $\omega < \omega_g$ and $\omega > \omega_d$, respectively [3]. R_i, C_g, C_{ds} and R_{ds} are shown in Fig. 2.

The characteristic impedance of this artificial line is frequency dependent and drops to 0 at cut-off. But, still large bandwidths are obtainable. For a given FET, its input and output capacitances are known. Then, the problem is to find an optimum (Z_0, ω_c) pair that maximizes the bandwidth of an artificial line. Note that, this optimum (Z_0, ω_c) pair depends on the reference impedance level(e.g., 50Ω), and the bandwidth definition (e.g, return loss greater than 10 dB). The gate capacitance of a MESFET is larger than the drain capacitance, so the bandwidth of the gate-line is narrower than the bandwidth of the drain-line, and determines the overall bandwidth of the amplifier. Thus, the gate-line design must be done first. Then, the drain-line must be designed to match the load, and the phase shifts of the gate and drain lines must be equalized.

The gate and drain-lines must be terminated with resistive loads in order to have the unwanted signals dissipate on these resistive loads. Single resistors close to the artificial line impedances can do the termination job well.

The resistive losses are the causes of the attenuation in artificial lines. Hence, in gain determination the losses of the artificial lines can not be neglected. No matter how small the attenuation per section is, the total attenuation of a distributed amplifier increases geometrically with increasing number of sections. On the other hand, the gain of a distributed amplifier increases arithmetically (addition of the transconductances). When the artificial line losses are included, the gain of a distributed amplifier can be found as the product of two terms (under perfect load and termination conditions):

$$A = G_0 \times G_1$$

where

$$G_0 = \frac{N \cdot g_m / C_d}{(1/x_d + \sqrt{1 - x^2})\sqrt{1 + x_g^2 x^2}} \cdot \frac{1}{\omega_c}$$

$$G_1 = \frac{1}{N} \cdot e^{-\frac{N-1}{2}(A_g + A_d)} \cdot \frac{\sinh(N \cdot (A_g - A_d)/2)}{\sinh((A_g - A_d)/2)}$$

where $x_d = \omega_c/\omega_d$, $x_g = \omega_g/\omega_c$, g_m is the transconductance of the FETs, C_d is the total drain capacitance, A_g and A_d are the attenuation per unit section of the gate and drain-lines and N is the number of sections.

Due to the geometric increase of the attenuation, there exists an optimum number of sections, N, which maximizes the gain. The optimum number of sections is found as [3]:

$$N_{opt} = \frac{\ln(A_g/A_d)}{A_g - A_d} \quad (2)$$

By adding small capacitances to the drains of the FETs we can have a control over ω_d, the lower end of the bandwidth.

3. DESIGNS AND LAYOUTS

Following the guidelines given above, the first design shown in Fig. 1 is implemented. This amplifier uses four identical sections although the optimum number of sections is found to be 6. Using a smaller number of sections than the optimum number gives a better gain flatness. About 5.5 dB gain is obtained in the 2-18 GHz range. The layout of this amplifier is shown in Fig. 3. The simulation results are shown in Fig. 4 and Fig. 5.

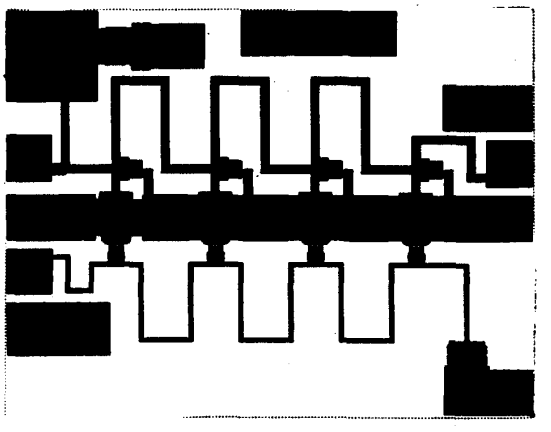

Fig. 3: Layout of the First Amplifier

This amplifier has been fabricated using GEC-Marconi's F20 Foundry Process. This process utilizes 0.5 micron gate-length. The fabricated chip is measured using an RF probe station and a network analyzer. The measurement results are shown in Fig. 6 and Fig. 7.

To obtain larger gain we need FETs with larger transconductances. This can be obtained from larger FETs. But, larger FETs have larger gate capacitances which means narrower bandwidth. Nevertheless, there is way of increasing the gain without decreasing the bandwidth. The high frequency end of the bandwidth is determined by the gate-line, and dominantly by the

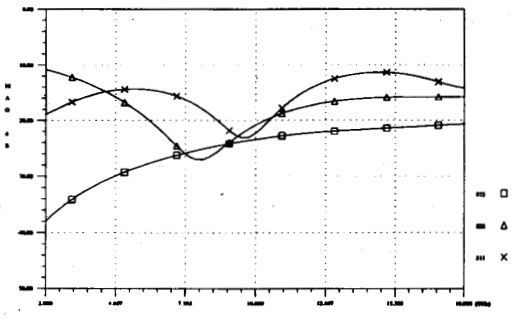

Fig. 4: Return Losses and Isolation of the First Amplifier

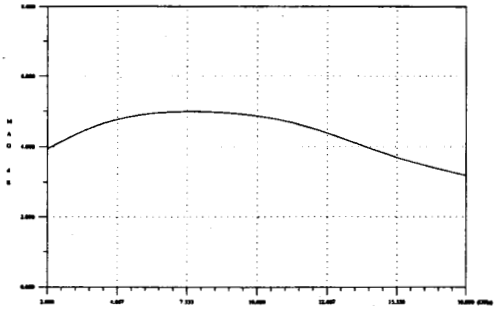

Fig. 5: Gain of the First Amplifier

first section. Keeping the first FET small and using larger FETs in the other sections increases the effective transconductance. Besides, the last section can be designed with a characteristic impedance to match the load and the previous sections with a higher characteristic impedance to increase gain [1].

The gain flatness is very much related to the phase delay relations of the gate and drain-line sections. Adding short sections of transmission lines in series with the drains of the FETs gives us a control over

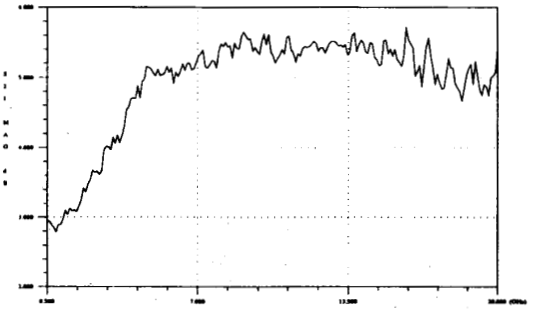

Fig. 6: Measured S_{21}

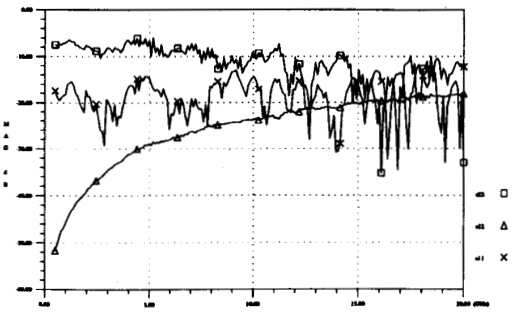

Fig. 7: Measured S_{11}, S_{22} and S_{12}

the phase delay of each section. By computer optimization the lengths of these transmission lines can be optimized to give a very flat gain response. Using these considerations another amplifier is designed and fabricated. This amplifier has the same structure with the first one, as shown in Fig. 8, but has an improved gain response (~6.5 dB). The gain of this amplifier is plotted in Fig. 9.

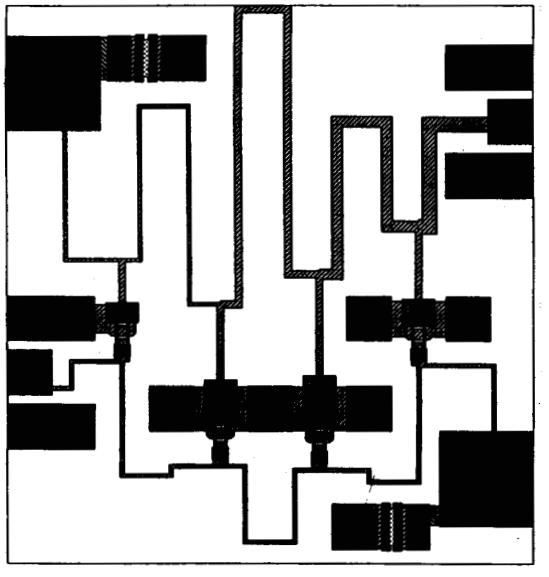

Fig. 8: Layout of the Second Amplifier

In a distributed amplifier, the gain is closely related to the output impedance of the active device. Since the output impedance of the device is in parallel with the voltage controlled current source, the higher the output impedance is, the higher output voltage we obtain. Cascode connection (shown in Fig. 10) is a way of increasing the output impedance of the active device [2]. Using cascode connected FETs the third am-

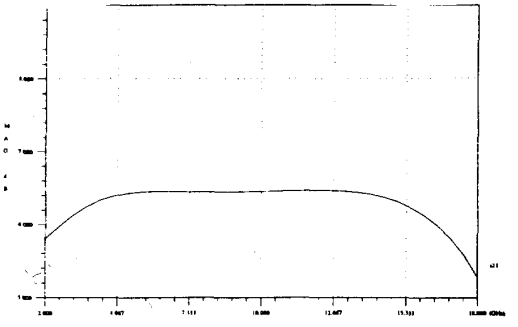

Fig. 9: Gain of the second design

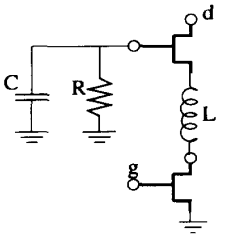

Fig. 10: Cascode connected FETs

plifier shown n Fig. 11 have been designed and fabricated. The bandwidth of this amplifier extends to 20 GHz and the gain is increased to 10.5 dB (Fig. 12). Another advantage of cascode connection is the increase in the isolation of the amplifier (greater than 35 dB).

4. CONCLUSION

Three distributed amplifiers have been designed and fabricated. The first of these fabricated amplifiers have been received and measured. The results show that the fabricated chip operates as a distributed amplifier, and works well up to 20 GHz.

ACKNOWLEDGEMENT

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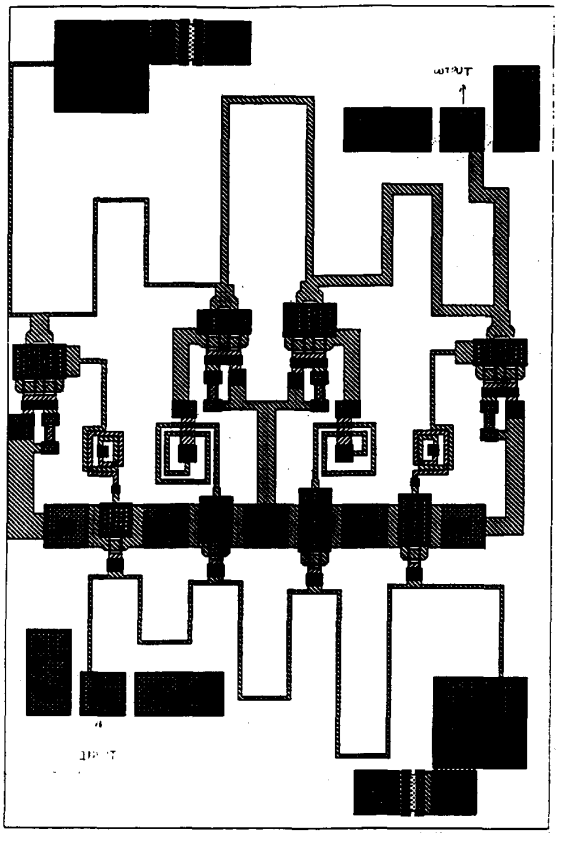

Fig. 11: Layout of the Third Amplifier

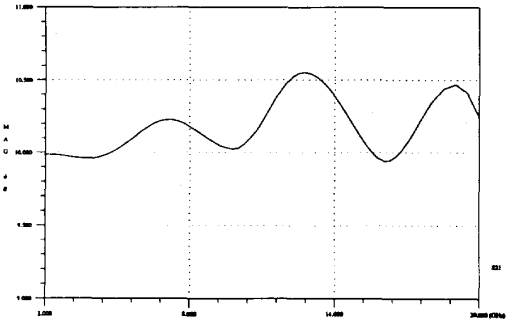

Fig. 12: Gain of the third design

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